Abstracts

A GaAs MMIC Based Successive Detection Logarithmic Amplifier (1992 Vol. I [MWSYM])

D.J. Nelly and D.S. Parsons. "A GaAs MMIC Based Successive Detection Logarithmic Amplifier (1992 Vol. I [MWSYM])." 1992 MTT-S International Microwave Symposium Digest 92.1 (1992 Vol. I [MWSYM]): 183-185.

A six stage successive detection logarithmic amplifier (SDLA) is described in which each stage is a GaAs Monolithic Microwave Integrated Circuit (MMIC) incorporating RF amplification, detection and a novel video summation technique, using standard 0.5 micron process field effect transistors (FET) and schottky diodes. The circuit has a dynamic range of 80 dB at 3.8 GHz with linearity of ±1 dB and power dissipation of 4.0 W.

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